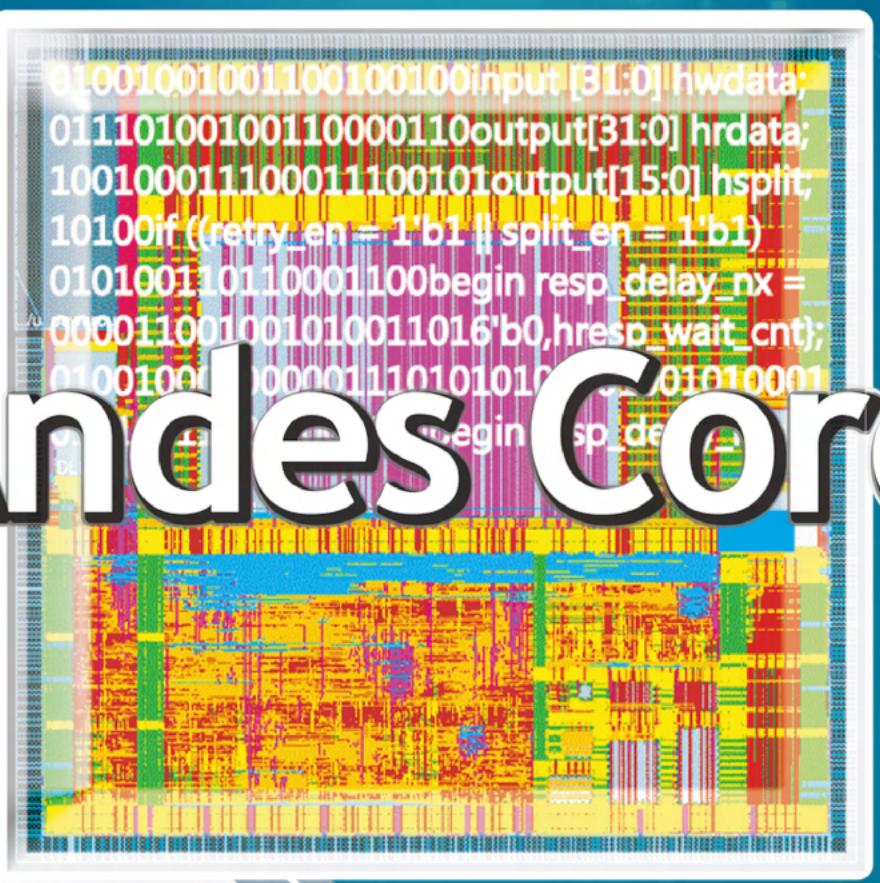


Andes Core™

ANDES TECHNOLOGY

Driving Innovations™

RISC-V®

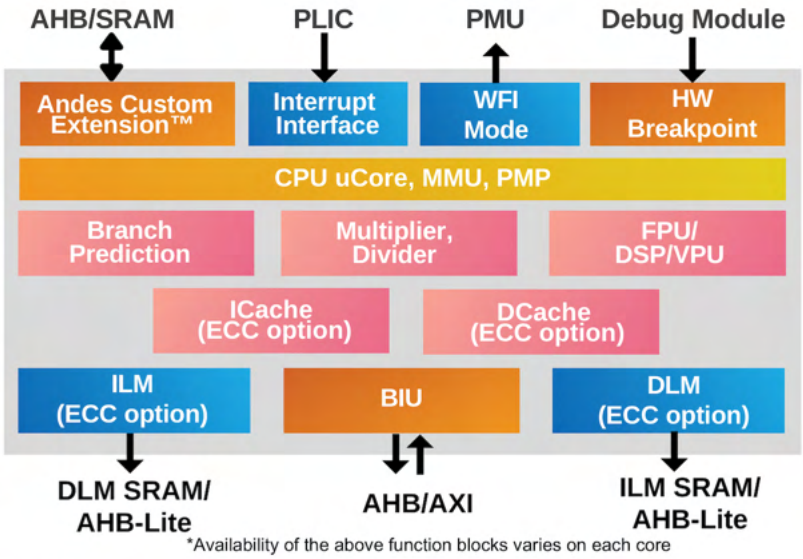
Andes Website

AndeStar™ Architecture

The AndeStar™ V5, the latest generation of Andes architecture, consists of both 32-bit and 64-bit register architectures with mixed-length 16/32-bit instructions. It adopts the RISC-V technology as its subset and benefits from the fast growing RISC-V ecosystem. Together with the merits of performance enhancement extensions ingerited from V3, the third generation RISC-style architecture, the AndeStar™ V5 brings compact, modular and customizable advantages to SoC applications. As a founding Premier member of the RISC-V International Association, Andes is determined to take RISC-V to the mainstream.

AndesCore™

AndesCore™ is a series of high performance CPU core families geared to diverse market segments of today's emerging embedded applications. The versatile and rich features of the AndesCore™ families allow flexible SoC customizations based on the application needs in a design to improve platform performance and reduce system cost. In addition, the processors employ various commonly-used low power design techniques to save energy and further allow smart SoC level power management for better energy/performance outcome.



*Availability of the above function blocks varies on each core

AndesCore™: The Leading RISC-V CPU IPs

	RISC-V CPU Cores+	Pipeline Stage	Best DMIPS (/MHz)%	Best CoreMark (/MHz)	Max Freq.*
22 / 23 Series	**N225** 32-bit Efficient and Compact	3	1.92	4.05	≥ 800 MHz
	D23 32-bit Efficient and Compact, DSP, Security	3	2.08	4.55	≥ 800 MHz
25 Series	**N25F / D25F / A25 / A25MP** 32-bit Fast and Compact, DSP, Linux, Multicore	5	1.98	3.57	≥ 1.1 GHz
	NX25F / AX25 / AX25MP 64-bit Fast and Compact, DSP, Linux, Multicore	5	2.14	3.55	≥ 1.1 GHz
27 Series	**A27 / A27L2** 32-bit MemBoost, Linux, L2 Cache	5	1.98	3.57	≥ 1.1 GHz
	AX27 / AX27L2 64-bit MemBoost, Linux, L2 Cache	5	2.14	3.55	≥ 1.1 GHz
45 Series	**N45 / D45 / A45 / A45MP** 32-bit Superscalar, DSP, Linux, Multicore	8	2.96	5.87	≥ 1.6 GHz
	NX45 / AX45 / AX45MP 64-bit Superscalar, DSP, Linux, Multicore	8	3.39	5.86	≥ 1.6 GHz
60 Series	**AX65** 64-bit Out-of-Order, Linux, Multicore	13	4.9	9.25	≥ 2.4 GHz
Vector Series	**NX27V** 64-bit MemBoost, 512-bit Vector	5	2.14	3.55	≥ 1.2 GHz
	AX45MPV 64-bit Superscalar, 1024-bit Vector, Linux, Multicore	8	3.39	5.86	≥ 1.41Ghz
FuSA Series	**D23-SE:** Compact, DSP, Security, ASIL-D complaint	3	2.08	4.55	≥ 800 MHz
	N/D25F-SE: Fast and Compact, DSP, ASIL-B compliant	5	1.91	3.57	≥ 1.0 GHz
	D45-SE: Superscalar, DSP, ASIL-D compliant	8	2.98	5.87	≥ 1.6 GHz

\+ **N**: Normal and Baseline; **D**: DSP; **A**: Linux; **MP**: Multicore; **V**: Vector; **L2**: L2 Cache; **SE**: Safety-Enhanced

% no-inline ground rules

★ All following data with I/O constraint
22/23 Series Synthesis with 28nm slow silicon, 0.9Vdd -40°C.
25/27 Series Synthesis with 28nm slow silicon, 0.9Vdd -40°C.
45 Series Synthesis with 7nm ULVT/LVT/SVT ssgnp 0.675v -40°C.
65 Series Synthesis with 7nm TT 0.75v 85 °C.
Vector Series NX27V Synthesis with 7nm 0.675v 0°C; AX45MPV Synthesis with 7nm ssgnp 0.675v -40 °C.
FuSa Series N/D25F-SE Synthesis with 28nm; D23-SE and D45-SE are estimated with 7nm.
Data are subject to change without notice.

\# Contact Andes for details.

ANDES TECHNOLOGY RISC-V®

AndesAIRE™: Andes AI Runs Everywhere

AndesAIRE™ AnDLA™: Andes Deep Learning Accelerator

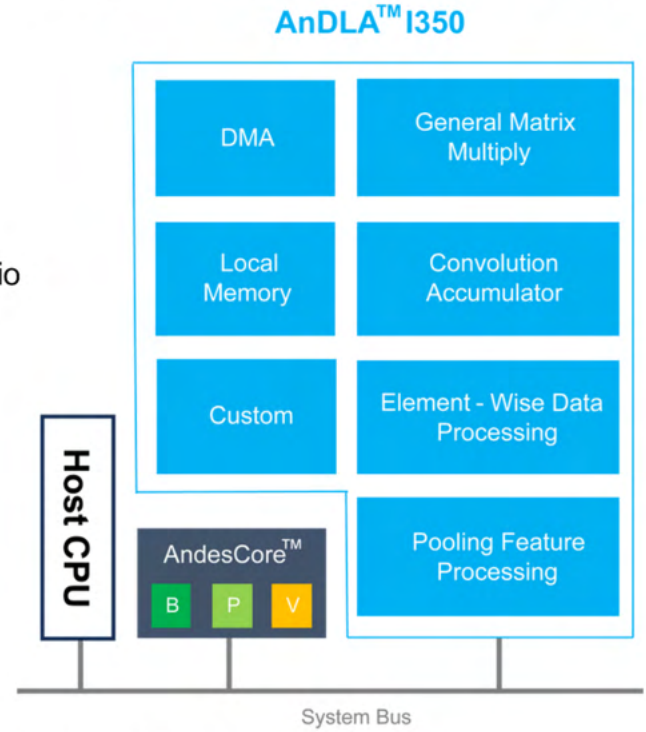
AndesAIRE™ AnDLA™ I350 is a deep learning accelerator (DLA) designed to enable high performance-efficient and cost-sensitive AI solutions for edge and end-point inference. It supports popular deep learning frameworks, such as TensorFlow Lite, PyTorch, and ONNX, and performs versatile neural network operations such as convolution, fully-connect, element-wise, activation, pooling, channel padding, upsample, concatenation, etc. in the int8 data type. It also features an internal Direct Memory Access (DMA) and local memory, utilizing the best computing power of the hardware engines. The key configurable parameters of **AnDLA™ I350** include the MAC number from 32 to 4096, and SRAM size from 16KB to 4MB, and provide flexible computing power from 64 GOPS to 8 TOPS (at 1 GHz) for a wide range of applications.

Features

- Configurable MACs from 32 to 4096 (INT8)
- Maximum performance 8 TOPS at 1GHz
- Configurable local memory: 16KB to 4MB
- Multi-dimension DMA
- Four 64-bit AXI bus interfaces
- NN applications: image / video, speech / voice / audio
- Accelerated rich NN operators and operator fusion

Applications

- AIoT device / TinyML on edge and end-point
- Smart camera
- Smart sensor
- Sensor hub
- Wearable
- Smart home appliance
- Robotic



AndesAIRE™ NN SDK:

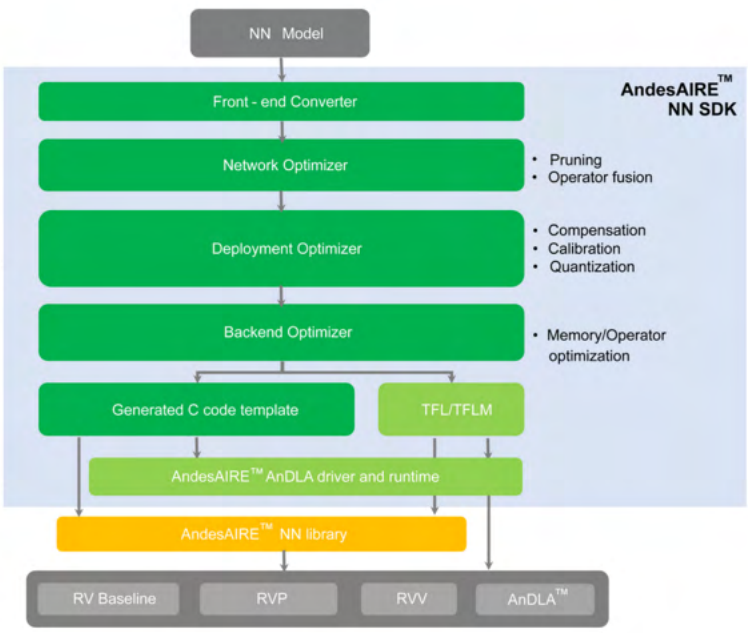
Software Tools / Runtimes for Development / Deployment

AndesAIRE™ NN SDK is a collection of software tools, libraries, runtimes, and sample programs for end-to-end development and deployment of **AndesAIRE™ AnDLA™** (Andes Deep Learning Accelerator) and **AndesCore™ RISC-V CPU** platforms. It includes the following components:

- **AndesAIRE™ NNPilot™**: a neural network optimization tool suite
- **AndesAIRE™ TFLM** (TensorFlow Lite for Microcontrollers): an optimized inference framework running on a host
- AnDLA™ driver and runtime

Features

- Input NN model formats: PyTorch, ONNX, TensorFlow Lite
- Network optimizer:
  - Pruning ratio by model / layer
  - Structured pruning
  - HW-awareness: number of MACs, SRAM size
- Deployment optimizer:
  - Numerical compensation
  - Batch normalization fusion
- Backend optimizer:
  - Memory footprint optimization, scheduler, OPs fusion, redundant OPs remover
  - Performance estimation
- Generated C code template to invoke AnDLA™ driver and NN library APIs



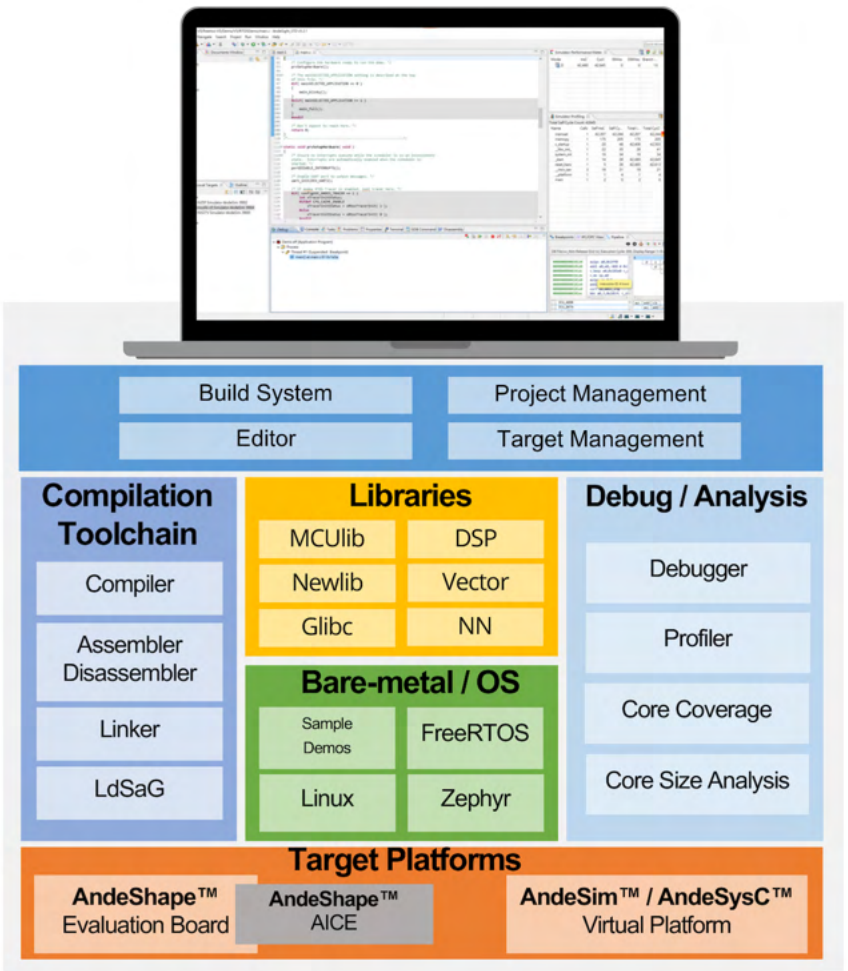
AndeSight™

Software Integrated Development Environment

AndeSight™ is a comprehensive Integrated Development Environment (IDE) which provides an efficient way to accelerate RISC-V application developments and easily boost the ultimate performance for AndesCore™ based SoCs.

Features

- Eclipse-based IDE
- User-friendly and easy-to-use environment
- Project and build system management
- Feature-rich editor
- Source code level debugger / profiling / code coverage / code size analysis
- RTOS awareness debugging
- In-System programming
- Multicore development support
- Highly-optimized toolchains for outstanding performance and compact memory footprint
- Abundant demos for boosting your development
- RTOS and Linux (LTP verified)
- Optimized C and compute libraries
- Peripheral drivers for AndeShape™ platform
- Near cycle-accurate simulator
- Arduino support for AndeShape™ Corvette EVB
- AICE debugger (4-wire/2-wire) with OpenOCD
- Windows / Ubuntu / CentOS / Red Hat



AndeSoft™

Board Support Package and Application Building Blocks

Andes provides a rich set of software components, from development tools, optimized C libraries, compute libraries, Real-Time Operating System, Linux kernel and drivers, middleware, to application framework, running on AndesCore™ processors under the name of AndeSoft™. Users can leverage those well-prepared and verified application building blocks and only focus on the tackling products to improve time-to-market.

Fundamental

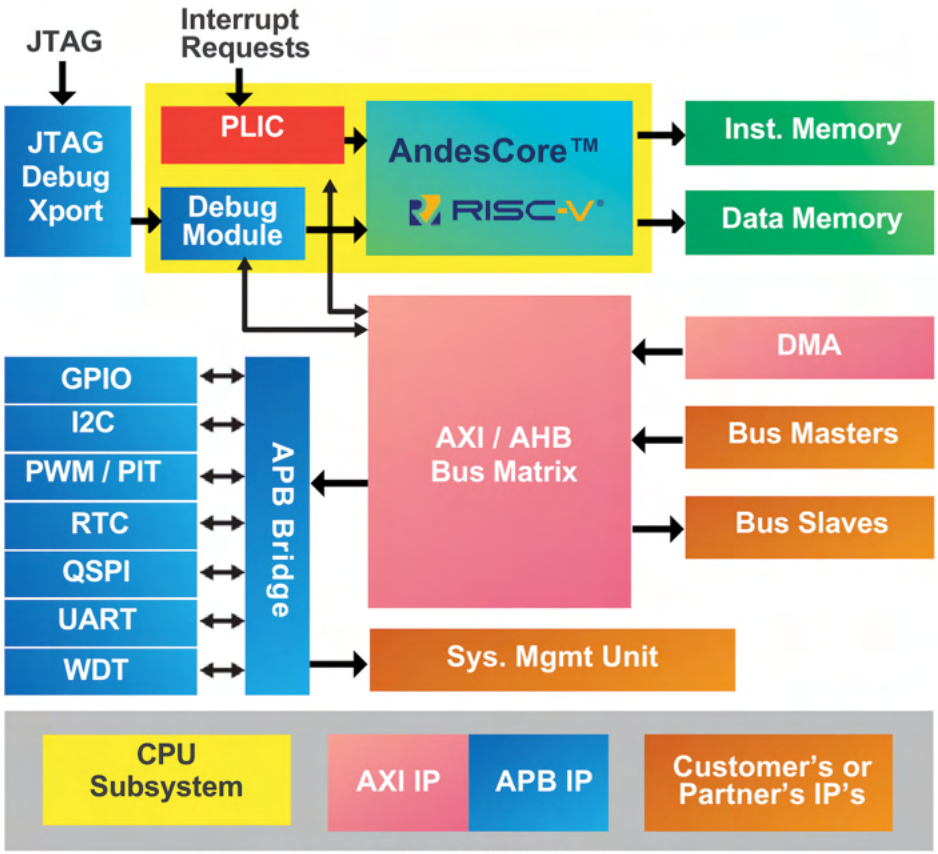
- Compiler/Toolchain are contributed to and supported officially by **GNU/LLVM** communities
- Debugging: **GDB and ICEman (speed-optimized OpenOCD)**
- Concise linker script and its tools, **Linker Scattering-and-Gathering (LdSaG)**
- Fast and near cycle-accurate simulators/models: **AndeSim™, AndeSysC™, Qemu**
- Optimized C library: **MCUlib**, newlib and glibc
- Optimized low-level compute libraries for DSP and vector processing: **libdsp, libvec, libnn**
- **Bare-metal drivers and demo programs** to demo AndesCore™ features

Operating Systems / Middleware / SW Framework

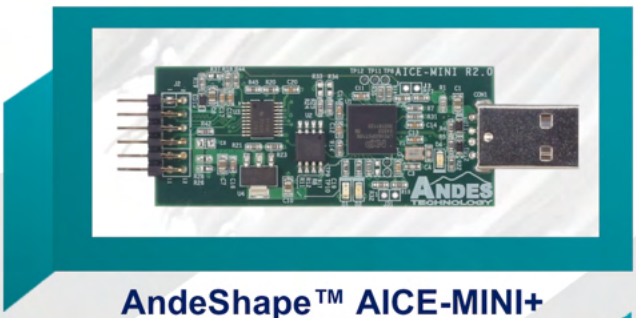
- RTOS: **FreeRTOS (RV32/64 UP)** aws qualified device, **Zephyr (RV32/64 UP/SMP), Azure ThreadX, and more**
- Linux kernel: **upstream compatible** and **in-house kernel** (v4.17/v5.4/v6.1/etc; LTS based; LTP verified, SMP)
- Drivers and advanced features: **strace**, **ftrace**, **Perf**, **SMU**, **power throttling**, **suspend-to-RAM, CPU hotplug, HIGHMEM** and **kernel module**
- **U-Boot, U-Boot-SPL, OpenSBI** and **BBL**

AndeShape™

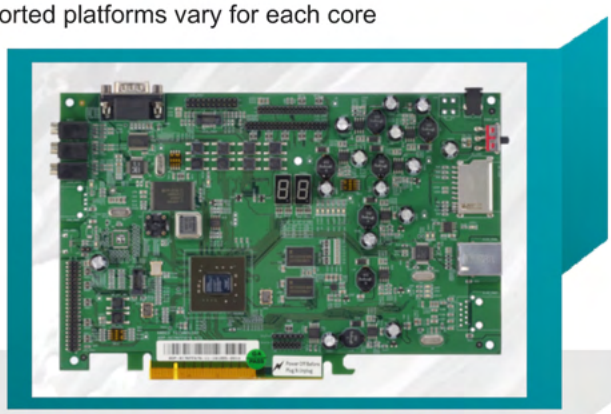
The AndeShape™ development platform includes variety of hardware entitles, such as pre-integrated IPs, ICE debuggers (AICE), and hardware evaluation boards for AndesCore™ processor based system development. To satisfy the best quality-of-result (QoR) requirements for different system applications, various platform IPs are available with different bus and datapath structures. In addition to a basic set of connectivity and storage devices, the rich set of hardware options in both board and SoC levels enable versatile flexibility in hardware/software co-development and early prototyping. The comprehensive debugging support, including in-system programming, self-diagnosis, and embedded ICE, greatly reduces the system development cycle while maintaining the quality of design.



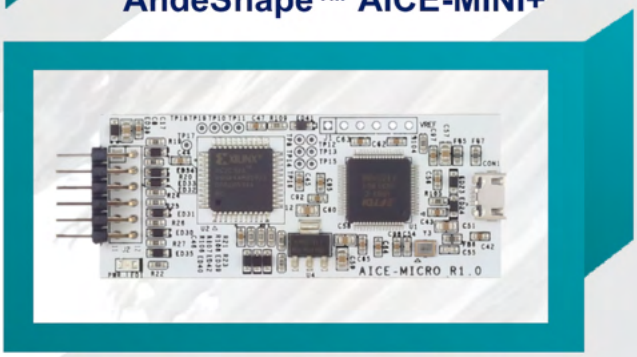
*Platform is pre-integrated with CPU subsystem
*Supported platforms vary for each core



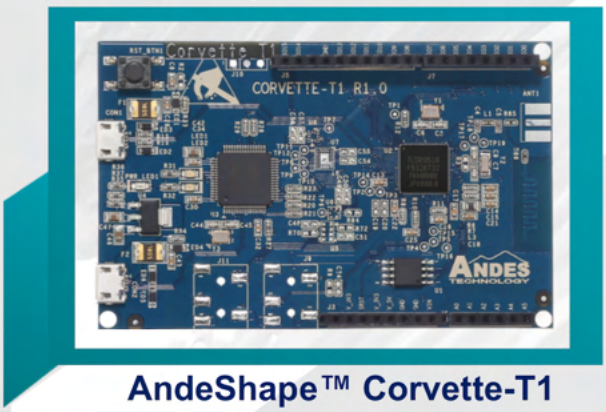
AndeShape™ AICE-MINI+



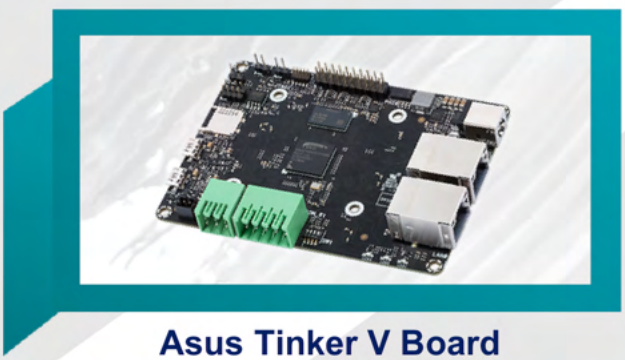
AndeShape™ ADP-XC7K160



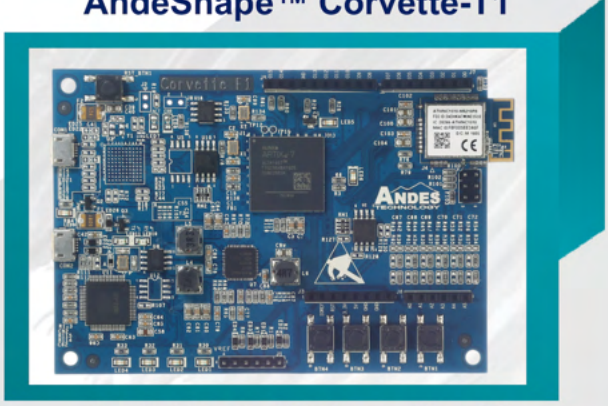
AndeShape™ AICE-MICRO



AndeShape™ Corvette-T1



Asus Tinker V Board



AndeShape™ Corvette-F1

About Andes Technology

Andes Technology, a Founding Premier member of RISC-V International and publicly listed CPU IP provider (TWSE: 6533; SIN: US03420C2089; ISIN: US03420C1099), has been devoting to the development of innovative high-performance/low-power 32/64-bit processors and associated SoC platforms since its foundation in 2005. Its powerful CPU lineup covering entry-level, mid-range, high-end, extensible and security families has achieved design wins in numerous embedded applications across the world, making a cumulative record of over 12 billion SoC shipment containing Andes IP as of 2022. While delivering advanced features based on proprietary ISAs, Andes also provides customized CPU service. For more information, please visit www.andestech.com.

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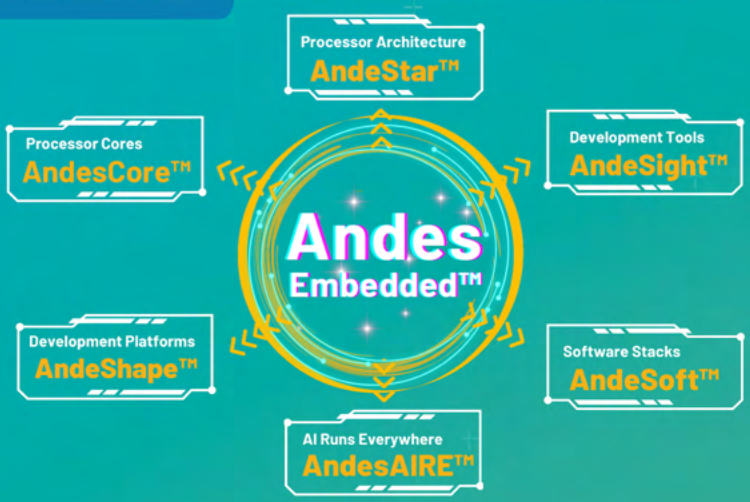

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